In the Claims

Please amend claim 14 as shown in the following detailed claim listing. Claim 14 is amended as to formatting only.

1. (Original) An integrated circuit comprising:

a processor comprising an instruction register to store a plurality of instructions, and a program counter to successively store a plurality of instruction identifiers each corresponding to a memory test instruction to be executed by the processor;

a first first-in-first-out (FIFO) store coupled to the program counter to store a number of instruction identifiers;

a memory coupled to the processor, the memory comprising a plurality of memory elements;

an address register to successively store a plurality of addresses each corresponding to a memory block comprising a number of the memory elements;

a second first-in-first-out (FIFO) store coupled to the address register to store a number of addresses; and

a storage element coupled to the memory to store a single memory block..

2. (Original) The integrated circuit recited in claim 1 wherein the memory elements are arranged in an M x N array, M and N being positive integers, and wherein a memory block comprises N memory elements.

3. (Original) The integrated circuit recited in claim 1 wherein the memory elements are arranged in an M x N array, M and N being positive integers, and wherein the storage element comprises N flip-flops.

4. (Original) The integrated circuit recited in claim 1 wherein the address register additionally successively stores a plurality of commands each corresponding to a memory block, and wherein the second first-in-first-out (FIFO) store additionally stores a number of commands.

5. (Original) An electronic assembly comprising:

a first integrated circuit including:

a processor comprising an instruction register to store a plurality of instructions, and a program counter to successively store a plurality of instruction identifiers each corresponding to a memory test instruction to be executed by the processor;

a first first-in-first-out (FIFO) store coupled to the program counter to store a number of instruction identifiers;

a memory coupled to the processor, the memory comprising a plurality of memory elements;

an address register to successively store a plurality of addresses each corresponding to a memory block comprising a number of the memory elements;

a second first-in-first-out (FIFO) store coupled to the address register to store a number of addresses; and

a storage element coupled to the memory to store a single memory block; and

an additional memory on at least one additional integrated circuit, the additional memory being coupled to the storage element.

6. (Original) The electronic assembly recited in claim 5 wherein the memory elements are arranged in an M x N array, M and N being positive integers, and wherein a memory block comprises N memory elements.

7. (Original) The electronic assembly recited in claim 5 wherein the memory elements are arranged in an M x N array, M and N being positive integers, and wherein the storage element comprises N flip-flops.

8. (Original) The electronic assembly recited in claim 5 wherein the address register additionally successively stores a plurality of commands each corresponding to a memory block, and wherein the second first-in-first-out (FIFO) store additionally stores a number of commands.

9. (Original) An electronic system comprising an electronic assembly having an integrated

circuit package comprising:

a processor comprising an instruction register to store a plurality of instructions, and a program counter to successively store a plurality of instruction identifiers each corresponding to a memory test instruction to be executed by the processor;

a first first-in-first-out (FIFO) store coupled to the program counter to store a number of instruction identifiers;

a memory coupled to the processor, the memory comprising a plurality of memory elements;

an address register to successively store a plurality of addresses each corresponding to a memory block comprising a number of the memory elements;

a second first-in-first-out (FIFO) store coupled to the address register to store a number of addresses; and

a storage element coupled to the memory to store a single memory block.

10. (Original) The electronic system recited in claim 9 and further comprising an additional memory on at least one additional integrated circuit package, the additional memory being coupled to the storage element.

11. (Original) The electronic system recited in claim 9 wherein the memory elements are arranged in an M x N array, M and N being positive integers, and wherein a memory block comprises N memory elements.

12. (Original) The electronic system recited in claim 9 wherein the memory elements are arranged in an M x N array, M and N being positive integers, and wherein the storage element comprises N flip-flops.

13. (Original) The electronic system recited in claim 9 wherein the address register additionally successively stores a plurality of commands each corresponding to a memory block, and wherein the second first-in-first-out (FIFO) store additionally stores a number of commands.

14. (Currently Amended) A data processing system comprising:

a bus coupling components in the data processing system;

a display coupled to the bus;

external memory coupled to the bus; and

an electronic assembly having an integrated circuit package including:

a processor comprising an instruction register to store a plurality of instructions, and a program counter to successively store a plurality of instruction identifiers each corresponding to a memory test instruction to be executed by the processor;

a first first-in-first-out (FIFO) store coupled to the program counter to store a number of instruction identifiers;

a memory coupled to the processor, the memory comprising a plurality of memory elements;

an address register to successively store a plurality of addresses each corresponding to a memory block comprising a number of the memory elements;

a second first-in-first-out (FIFO) store coupled to the address register to store a number of addresses; and

a storage element coupled to the memory to store a single memory block.

15. (Original) The data processing system recited in claim 14 wherein the external memory resides on at least one additional integrated circuit package that is coupled to the storage element.

16. (Original) The data processing system recited in claim 14 wherein the memory elements are arranged in an M x N array, M and N being positive integers, and wherein a memory block comprises N memory elements.

17. (Original) The data processing system recited in claim 14 wherein the memory elements

are arranged in an M x N array, M and N being positive integers, and wherein the storage element comprises N flip-flops.

18. (Original) The data processing system recited in claim 14 wherein the address register additionally successively stores a plurality of commands each corresponding to a memory block, and wherein the second first-in-first-out (FIFO) store additionally stores a number of commands.

19. (Original) A method of testing a memory comprising a plurality of memory elements, the method comprising:

performing a plurality of tests, including read tests, on the memory in accordance with a sequence of instructions, the instructions each being uniquely identified by a corresponding instruction identifier, each test comprising an address corresponding to a memory block, and each read test resulting in a memory block being read;

generating a memory fault signal when one of the read tests fails; and

in response to the memory fault signal, storing an address corresponding to the one read test, storing several subsequent addresses, and storing a read memory block corresponding only to the one read test.

20. (Original) The method recited in claim 19 wherein the memory is a component of an integrated circuit that further comprises a processor.

21. (Original) The method recited in claim 19 wherein each test additionally comprises a command, and wherein a command is concurrently stored whenever an address is stored.

22. (Original) The method recited in claim 19 and further comprising:

in response to the memory fault signal, storing an instruction identifier corresponding to the one read test, and further storing several subsequent instruction identifiers.

23. (Original) The method recited in claim 22 wherein the instructions reside in an instruction register, and wherein each instruction identifier comprises a program counter value.

24. (Original) The method recited in claim 22 and further comprising:

retrieving the instruction identifier corresponding to the one read test;

executing a sequence of instructions up to and including an instruction identified by the instruction identifier corresponding to the one read test; and

storing the read memory block corresponding to the one read test to another memory.

25. (Original) The method recited in claim 24 wherein the memory is a component of an integrated circuit that further comprises a processor, and wherein the another memory is not located on the integrated circuit.

26. (Original) The method recited in claim 24 wherein in the executing operation the sequence of instructions are executed at the normal operational speed of the memory being tested.

27. (Original) The method recited in claim 24 and further comprising:

incrementing the instruction identifier by one count, resulting in an incremented instruction identifier;

executing a sequence of instructions up to and including an instruction identified by the incremented instruction identifier; and

storing a read memory block corresponding to a test immediately subsequent to the one read test to the another memory.

28. (Original) The method recited in claim 27 and further comprising:

examining the stored read memory blocks and the stored addresses to isolate the location of one or more faulty memory elements in the memory being tested.

29. (Original) The method recited in claim 24 and further comprising:

incrementing the instruction identifier by one count, resulting in an incremented instruction identifier;

executing an instruction identified by the incremented instruction identifier; and

storing a read memory block corresponding to a test immediately subsequent to the one read test to the another memory.

30. (Original) The method recited in claim 29 and further comprising:

examining the stored read memory blocks and the stored addresses to isolate the location of one or more faulty memory elements in the memory being tested.

Amendments to the Specification

Applicants have made several amendments to the specification by deleting wording that refers to the "invention" without referring to one or more embodiments of the invention , and by substituting "embodiments of the invention" or "subject matter" for "invention" or "present invention". This is because Applicants do not wish the claims to be interpreted as being limited to a single "invention". No new matter has been added by way of these amendments to the specification.

Amendments to Claim 14

Claim 14 has been amended as to formatting only. No new matter has been introduced.

The amendment to claim 14 is made to satisfy Applicants' preferences, not necessarily to satisfy any legal requirement(s) of the patent laws, and it is not intended to limit the scope of equivalents to which any claim element may be entitled.

Conclusion

It is respectfully submitted that these changes do not introduce new matter, and the claims are allowable without further search or consideration. Therefore, entry is appropriate under Rule 312 and is respectfully requested. The Examiner is invited to telephone Applicants' Attorney, Walter W. Nielsen at (602) 298-8920, or the below-signed attorney to facilitate prosecution of this application.

Respectfully submitted,

NGUYEN N. NGO ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
612-349-9592

Date: July 11, 2003 By: Ann M. McCrackin

Ann M. McCrackin
Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 11 day of July, 2003.

Name: ANN MCCRACKIN Signature: Ann M. McCrackin